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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/484,961	NOWELL ET AL.	
	Examiner	Art Unit	
	Frank Duong	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-66* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is a response to communications dated 07/03/06. Claims 1-66 are pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-66 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshikawa et al (Skewless Optical Data-Link Subsystem for Massively Parallel Processors Using 8 Gb/s X 1.1 Gb/s MMF Array Optical Module) (hereinafter "Yoshikawa").

Regarding **claim 1**, in accordance Yoshikawa reference entirety, Yoshikawa discloses a system (Figure 1) for transferring synchronous optical network/synchronous digital hierarchy (SONET/SDH) frames (48 bit X 100 Mb/s) between a first and second node (*Fig. 1 depicted subsystems*) comprising:

a demultiplexer (*Fig. 1; Input: 48 bit X 100Mb/s*) to map SONET/SDH frames onto a plurality of data channels (MMF ribbon) (*see Figure 1 and the corresponding description starting on page 1625, section II*);

an encoder (*Fig. 1; 8b10b coder*) to encode and translate data onto each data channel for transmission (*page 1626, left column and description pertaining 8b10b coder*);

a first de-skewing processor (*Fig. 1; Sync pattern insertion*) to overwrite a frame marker on the SONET/SDH frames with a unique frame marker (*K28.5*) to aid in de-skewing the plurality of data channel (*page 1626, left column, Yoshikawa discloses Sync pattern, K28.5 generated by 8b10b coder, is inserted to skew compensate*);

a second de-skewing processor (*Fig.1; sync pattern extraction*) to de-skew the data from the plurality of data channels based on the unique frame marker (K28.5) and to restore the frame marker on the SONET/SDH channel (*page 1626, left column, Yoshikawa discloses when the sync pattern is detected, the detection timing is compared with that of the master channel and deskew operation is performed using FIFO memory to output data synchronous to the master channel*);

a decoder (*Fig. 1; 10b8b decoder*) to decode and translate data on each data channel for reception; and

a multiplexer (*Fig. 1; Output: 48 bit X 100Mb/s)* map the plurality of data channels (MMF ribbon) onto SONET/SDH frames (*see Figure 1 and the corresponding description* on page 1626).

Regarding **claim 2**, in addition to features recited in base claim 1 (see rationales discussed above), Yoshikawa further discloses wherein the multiplexer includes a framer (*not shown; inherent in 48 bit X 100 Mb/s component of Figure 1*) to determine the position of frame markers in the data (*see page 11625, right column, section II, Yoshikawa discloses 48 Mb/s X 100Mb/s of parallel data is grouped into 6 ch X 8 b. In grouping of data channels, it is inherently there is a step of determining the position of frame markers in the data*).

Regarding **claim 3**, in addition to features recited in base claim 1 (see rationales discussed above), Yoshikawa further discloses wherein the first and second nodes communicate over parallel transmission links (*Fig. 1; MMF ribbon*).

Regarding **claim 4**, in addition to features recited in base claim 2 (see rationales discussed above), Yoshikawa further discloses wherein the parallel transmission links comprise a parallel-optics based transmission link (*Fig. 1; MMF ribbon*).

Regarding **claim 5**, in addition to features recited in base claim 3 (see rationales discussed above), Yoshikawa further discloses wherein the parallel transmission link comprise a wavelength division multiplex (WDM) based transmission link (*Fig. 1; MMF ribbon*).

Regarding **claim 6**, in accordance Yoshikawa reference entirety, Yoshikawa discloses a method (*Figure 1*) for transferring synchronous optical network/synchronous digital hierarchy (SONET/SDH) frames between a first and second node *(Fig. 1 depicted transmitting and receiving subsystems*) comprising:

mapping (*Fig. 1; Input: 48 bit X 100Mb/s*) the SONET/SDH frames (48 Mb/s X 100Mb/s) onto a plurality of data channels (MMF ribbon) (*see Fig. 1 and description on page 1625, right column, section II*);

overwriting (*Sync pattern insertion*) a frame marker on the SONET/SDH frames with a unique frame marker (K28.5) to aid in de-skewing the plurality of data channels (MMF ribbon) (*page 1626, left column, Yoshikawa discloses Sync pattern, K28.5 generated by 8b10b coder, is inserted to skew compensate*); and

transferring (Fig. 1) the SONET/SDH frames over a plurality of parallel transmission links (MMF ribbon) (*see Fig. 1 and the corresponding description pertaining the 8 X 1 Gb/s array optical modules on page 1626, left column.*)

Regarding **claim 7**, in addition to features recited in base claim 6 (see rationales discussed above), Yoshikawa further discloses wherein transferring the SONET/SDH frames over parallel transmission links includes transmitting and receiving the SONET/SDH frames over parallel transmission links (*see Fig. 1; MMF ribbon*).

Regarding **claim 8**, in addition to features recited in base claim 7 (see rationales discussed above), Yoshikawa further discloses byte stripping of the SONET/SDH frames onto parallel data channels (*see Fig. 1 and the description on page 1626, left column pertaining the coded 6 X 10 bit data as 60:6 multiplexed and transmitted through a GI/62.5 MMF ribbon*).

Regarding **claim 9**, in addition to features recited in base claim 7 (see rationales discussed above), Yoshikawa further discloses encoding each data channel for data formatting (see Fig. 1; 8b10 coder).

Regarding **claim 10**, in addition to features recited in base claim 7 (see rationales discussed above), Yoshikawa further discloses framing each data channel (*see Fig. 1 and Input: 48 bit X 100Mbps*).

Regarding **claims 11-12**, in addition to features recited in base claim 6 (see rationales discussed above), Yoshikawa further discloses wherein the parallel transmission link comprises a 12 fiber (see Fig. 1 and MMF ribbon).

Regarding **claim 13**, in addition to features recited in base claim 6 (see rationales discussed above), Yoshikawa further discloses wherein the parallel transmission link comprises a wavelength division multiplex (WDM) based transmission link (see Fig. 1 and MMF ribbon).

Regarding **claim 14**, in addition to features recited in base claim 6 (see rationales discussed above), Yoshikawa further discloses wherein the rate of SONET/SDH frames corresponds to an OC-192/STM-64 line rate (*8 Gb/s*) (*see Fig. 1 and 8 X 1.1 Gb/s array E/O transceiver modules*).

Regarding **claim 15**, in addition to features recited in base claim 7 (see rationales discussed above), Yoshikawa further discloses wherein receiving SONET/SDH frames further comprises, receiving (Fig. 1; 8 X 1.1 Gb/s array O/E module) data from each of the parallel transmission links (MMF ribbon); decoding (10b8b decoder) each data channel; realigning (*Fig. 1; Sync pattern extraction*) each data channel to compensate for an inter-channel skew; and recombining the data channels into a SONET/SDH frame (ouput: 48 bit X 100Mbps).

Regarding **claim 16**, in accordance Yoshikawa reference entirety, Yoshikawa discloses a method (*Fig. 1*) for transferring synchronous optical network (SONET)/synchronous digital hierarchy (SDH) frames (*48bit X 400Mb/s*) over a parallel transmission system (*Fig. 1; Fiber Ribbon*) comprising:

mapping (*Fig. 1; Input: 48 bit X 100Mb/s*) the SONET/SDH frames (48 Mb/s X 100Mb/s) onto a plurality of data channels (MMF ribbon) (*see Fig. 1 and description on page 1625, right column, section II*);

overwriting (*Sync pattern insertion*) a frame marker on the SONET/SDH frames with a unique frame marker (K28.5) to aid in de-skewing the plurality of data channels (MMF ribbon) (*page 1626, left column, Yoshikawa discloses Sync pattern, K28.5 generated by 8b10b coder, is inserted to skew compensate*); and

transmitting (Fig. 1) the SONET/SDH frames over a plurality of parallel transmission links (MMF ribbon) (*see Fig. 1 and the corresponding description pertaining the 8 X 1 Gb/s array optical modules on page 1626, left column.*)

Regarding **claim 17**, in accordance Yoshikawa reference entirety, Yoshikawa discloses a method (*Fig. 1*) of transmitting SONET/SDH frames (*48bit X 400Mb/s*) having framer markers (*not shown; inherently there is A bit in the disclosed frames*), the method comprising:

determining the position of frame markers in the data (*see page 11625, right column, section II, Yoshikawa discloses 48 Mb/s X 100Mb/s of parallel data is grouped into 6 ch X 8 b. In grouping of data channels, it is inherently there is a step of determining the position of frame markers in the data*);

byte stripping of the SONET/SDH frames onto parallel data channels (*see Fig. 1 and the description on page 1626, left column pertaining the coded 6 X 10 bit data as 60:6 multiplexed and transmitted through a GI/62.5 MMF ribbon*);

encoding (Fig. 1; 8b10 coder) each data channel;

overwriting (*Sync pattern insertion*) a frame marker on the SONET/SDH frames with a unique frame marker (K28.5) to aid in de-skewing the plurality of data channels

(MMF ribbon) (*page 1626, left column, Yoshikawa discloses Sync pattern, K28.5 generated by 8b10b coder, is inserted to skew compensate*); and

transmitting (Fig. 1) the SONET/SDH frames over a plurality of parallel transmission links (MMF ribbon) (*see Fig. 1 and the corresponding description pertaining the 8 X 1.1 Gb/s array optical modules on page 1626, left column.*)

Regarding **claims 18-19**, in addition to features recited in base claim 17 (see rationales discussed above), Yoshikawa further discloses wherein the parallel transmission link comprises a 12 fiber (*Fig. 1; MMF Ribbon*).

Regarding **claim 20**, in addition to features recited in base claim 17 (see rationales discussed above), Yoshikawa further discloses wherein the parallel transmission links comprises a wavelength division multiplex (WDM) based transmission link (*Fig. 1; MMF Ribbon*).

Regarding **claim 21**, in addition to features recited in base claim 17 (see rationales discussed above), Yoshikawa further discloses wherein the rate of SONET/SDH frames corresponds to an OC-192/STM-64 line rate (*8 Gb/s*) (*see Fig. 1 and 8 X 1.1 Gb/s array E/O transceiver modules*).

Regarding **claim 22**, in addition to features recited in base claim 17 (see rationales discussed above), Yoshikawa further discloses wherein frame delimiting is performed by overwriting at least a SONET byte on each data channel (*see page 1626, left column, Yoshikawa discloses skew was compensated using inserted sync pattern, which is a K28.5-characters generated in the 8b10b coding.*)

Regarding **claim 23**, in addition to features recited in base claim 17 (see rationales discussed above), Yoshikawa further discloses wherein at least a first three SONET framing bytes are overwritten on each data channel (*see page 1626, left column, Yoshikawa discloses skew was compensated using inserted sync pattern, which is a K28.5-characters generated in the 8b10b coding.*)

Regarding **claim 24**, in addition to features recited in base claim 17 (see rationales discussed above), Yoshikawa further discloses wherein unique frame delimiters are used on a subset of the data channels (*see page 1626, left column, Yoshikawa discloses skew was compensated using inserted sync pattern, which is a K28.5-characters generated in the 8b10b coding.*)

Regarding **claim 25**, in addition to features recited in base claim 24 (see rationales discussed above), Yoshikawa further discloses wherein a first, frame delimiter is used for a first half of the data channel and a second frame delimiter is used for a second half of the data channels (*see page 1626, left column, Yoshikawa discloses skew was compensated using inserted sync pattern, which is a K28.5-characters generated in the 8b10b coding.*)

Regarding **claim 26**, in addition to features recited in base claim 17 (see rationales discussed above), Yoshikawa further discloses wherein each channel is encoded using a block-code (*Fig. 1; 8b10 coder*).

Regarding **claim 27**, in addition to features recited in base claim 17 (see rationales discussed above), Yoshikawa further discloses wherein the data channels are logically combined in such a manner to enable recovery of a single data channel

and the logically combined channel exists as a separate data channel (*see Fig. 1; 8 X 1.1 Gb/s array transceiver modules*).

Regarding **claim 28**, in addition to features recited in base claim 17 (see rationales discussed above), Yoshikawa further discloses wherein a further data channel carries cyclic redundancy check (CRC) bits for the plurality of data channels (*see page 1626, right column pertaining monitoring the CRC bit at the receiving Switching Unit*).

Regarding **claim 29**, in accordance Yoshikawa reference entirety, Yoshikawa discloses a method (*Fig. 1)* of receiving SONET/SDH frames (*48bit X 100Mbps*) over a parallel transmission system (*Fig. 1*) comprising:

recovering (*8 X 1.1 Gb/s array O/E module*) data from each transmission link (MMF ribbon);

decoding (10b8b decoder) each data channel;

realigning (*Sync pattern extraction*) each data channel based on a unique marker (K28.5) to compensate for an inter-channel skew (*see page 1626, left column, Yoshikawa discloses when the sync pattern is detected, the detection timing is compared with that of the master channel and the deskew operation is performed using a FIFO memory*);

restoring the unique frame marker to a frame marker normally on the SONET/SDH frames (*see page 1626, left column, Yoshikawa discloses deskewing operation is performed using FIFO memory to output data synchronous to the master*

channel. In doing so, it is inherent the original data to include normal frame marker in the SONET frames is restored); and

recombining (*ouput: 48bit X 100Mb/s*) the data channels into a SONET/SDH frame (see Fig. 1).

Regarding **claims 30-31**, in addition to features recited in base claim 29 (see rationales discussed above), Yoshikawa further discloses wherein the parallel transmission link comprises a 12 fiber (*Fig. 1; MMF ribbon*).

Regarding **claim 32**, in addition to features recited in base claim 29 (see rationales discussed above), Yoshikawa further discloses wherein the parallel transmission links comprises a wavelength division multiplex (WDM) based transmission link (*Fig. 1; MMF ribbon*).

Regarding **claim 33**, in addition to features recited in base claim 29 (see rationales discussed above), Yoshikawa further discloses wherein the rate of SONET/SDH frames corresponds to an OC-192/STM-64 line rate (*8 Gb/s*) (*see Fig. 1 and 8 X 1.1 Gb/s array E/O transceiver modules*).

Regarding **claim 34**, in addition to features recited in base claim 29 (see rationales discussed above), Yoshikawa further discloses wherein the receiver detects a polarity of the transmission links by use of unique frame delimiters (K28.5-characters) on subset of the data channels (*see page 1626, left column pertaining the K28.5-characters and right column, last paragraph pertaining the CRC bit*).

Regarding **claim 35**, in addition to features recited in base claim 30 (see rationales discussed above), Yoshikawa further discloses a loss of synchronization

condition on a channel if a plurality of code word violation occurs (*see page 1626, right column pertaining CRC bit*).

Regarding **claim 36**, in addition to features recited in base claim 35 (see rationales discussed above), Yoshikawa further discloses wherein a channel failure is detected using the loss of synchronization condition (*see page 1626, right column pertaining CRC bit*).

Regarding **claim 37**, in addition to features recited in base claim 29 (see rationales discussed above), Yoshikawa further discloses detecting and correcting errors on the data channels by calculating a cyclic redundancy check for a block of data on the data channels; comparing the CRC to a corresponding, separately-transmitted CRC for the block; and recovering the data from a protection channel if the CRC's do not match (*see page 1626, right column, last paragraph pertaining CRC bit*).

Regarding **claim 38**, in accordance Yoshikawa reference entirety, Yoshikawa discloses a transceiver module (*Fig.1*) for transferring SONET/SDH frames (*48bit X 100Mbps*) between a first and second node (*see Fig. 1*), comprising:

a converter circuit (*Fig. 1; coder*) to adapt incoming signals (*48bit X 100Mbps*) for transmission on parallel transmission links (*MMF ribbon*);

a first de-skewing processor (*Fig. 1; Sync pattern insertion*) to overwrite a first frame marker on first SONET/SDH frames with a first unique frame marker (K28.5) to aid in de-skewing first data channels (MMF ribbon);

a parallel transmit optic module (*8 X 1.1 Gb/s array E/O module*) to transmit the first data channels on the parallel transmission links (*MMF ribbon*); and

a parallel receive optic module (*8 X 1.1 Gb/s array E/O module*) to receive second data channels on the parallel transmission links (*MMF ribbon*); and

a second de-skewing processor (*Fig. 1; Synch pattern extraction*) to de-skew data from the second data channels based on a second unique frame markers and to restore a second frame marker on second SONET/SDH frames (*see page 1626, left column, Yoshikawa discloses deskewing operation is performed using FIFO memory to output data synchronous to the master channel. In doing so, it is inherent the original data including normal frame marker in the SONET frames is restored*).

Regarding **claim 39**, in addition to features recited in base claim 38 (see rationales discussed above), Yoshikawa further discloses wherein a rate for transferring SONET/SDH frames corresponds to an OC-192/STM-64 line rate *8 Gb/s*) (*see Fig. 1 and 8 X 1.1 Gb/s array E/O transceiver modules*).

Regarding **claim 40**, in addition to features recited in base claim 38 (see rationales discussed above), Yoshikawa further discloses wherein the first and second node communicate over parallel transmission links (*Fig. 1; MMF Ribbon*).

Regarding **claim 41**, in addition to features recited in base claim 40 (see rationales discussed above), Yoshikawa further discloses wherein the parallel transmission links (*Fiber Ribbon*) comprises a parallel-optics based transmission link (*Fig. 1; MMF Ribbon*).

Regarding **claim 42**, in addition to features recited in base claim 40 (see rationales discussed above), Yoshikawa further discloses wherein the parallel

transmission links comprises a wavelength division multiplex (WDM) based transmission link (*Fig. 1; MMF Ribbon*).

Regarding **claim 43**, in addition to features recited in base claim 38 (see rationales discussed above), Yoshikawa further discloses wherein the converter circuit (coder) interfaces with a frame chip (*see Fig. 1; Input: 48 bit X 100Mb/s*).

Regarding **claim 44**, in addition to features recited in base claim 38 (see rationales discussed above), Yoshikawa further discloses wherein the parallel transmit optic module is integral with the parallel receive optic module (*see Fig. 1*).

Regarding **claim 45**, in addition to feature recited in base claim 1 (see rationales discussed above), Yoshikawa further discloses wherein the encoder overwrites the frame markers on each channel with unique frame markers used for automatic skew compensation (*see Fig. 1 and the corresponding description on page 1626, right column, discussed about K28.5-characters insertion for skew suppression or compensation*).

Regarding **claim 46**, in addition to feature recited in base claim 45 (see rationales discussed above), Yoshikawa further discloses wherein the unique frame markers (*K28.5-characters*) are different for each channel (*MMF ribbon*).

Regarding **claim 47**, in addition to feature recited in base claim 46 (see rationales discussed above), Yoshikawa inherently discloses a ribbon patch cord with multiple optical fibers because Fig. 4 shows the configuration of a parallel optical links having GI62.5 ribbon fiber as a testbed.

Regarding **claim 48**, in addition to feature recited in base claim 47 (see rationales discussed above), Yoshikawa further discloses an aligner (Fig. 1; Sync pattern extraction) that re-orders the channels based on the unique frame markers (K28.5-characters) to compensate for a crossover of optical fibers in the ribbon patch cord (*see page 1626, left column, Yoshikawa discloses a deskewing operation to compensate the skew using inserted sync pattern*).

Regarding **claim 49**, in addition to feature recited in base claim 47 (see rationales discussed above), Yoshikawa further discloses an aligner (Fig. 1; Sync pattern extraction) that re-orders on the channels as a function of the unique frame markers (K28.5-characters) (*see page 1626, left column, Yoshikawa discloses a deskewing operation to compensate the skew using inserted sync pattern*).

Regarding **claim 50**, in addition to feature recited in base claim 1 (see rationales discussed above), Yoshikawa further discloses an aligner (*Fig. 1; Sync pattern extraction*) that deskews individual channels by using the unique frame marker as delimiters to compensate for inter-channel skew that occurs due to propagation delay differences between or among the channel (*see page 1626, left column, Yoshikawa discloses a deskewing operation to compensate the skew using inserted sync pattern*).

Regarding **claim 51**, in addition to features recited in base claim 1 (see rationales discussed above), Yoshikawa further discloses wherein the data channels are logically combined in such a manner to enable recovery of a single data channel and the logically combined channel exists as a separate data channel (*see Fig. 1; 10:1 multiplex*).

Regarding **claim 52**, in addition to features recited in base claim 1 (see rationales discussed above), Yoshikawa further discloses wherein a further data channel carries cyclic redundancy check (CRC) bits for the plurality of data channels (*see page 1626, right column, last paragraph pertaining CRC bit*).

Regarding **claim 53**, in addition to features recited in base claim 1 (see rationales discussed above), Yoshikawa further discloses wherein the de-skewing process (Sync pattern insertion) is integrated with the converter circuit (coder) (see Fig. 1).

Regarding **claim 54**, in addition to features recited in base claim 1 (see rationales discussed above), Yoshikawa further discloses wherein the first de-skewing processor (Sync pattern insertion) and second de-skewing processor (Sync pattern extraction) are the same processor (see Fig. 1).

Regarding **claim 55**, in accordance with Yoshikawa reference entirety, Yoshikawa discloses a system (Fig. 1) for transferring synchronous optical network/synchronous digital hierarchy (SONET/SDH) frames (48bit X 100Mb/s), the system comprising:

a demultiplexer (Input: 48 bit X 100Mb/s) to map incoming frames of data having a given number of bits onto a plurality of data channels in a manner supporting de-skewing the data from the data channels (MMF ribbon) without increasing the given number of bits on the data channels (*see page 1626, right column pertaining the insertion of sync pattern to compensate for skewing*); and

a de-skewing processor (*Fig. 1; Sync pattern extraction*) to de-skew the data from the data channels (MMF ribbon) based on the mapped incoming frames (*see page 1626, right column pertaining the extraction of sync pattern performed by the deskewing operation*).

Regarding **claim 56**, in addition to features recited in base claim 55 (see rationales discussed above), Yoshikawa further discloses wherein the demultiplexer includes a framer to determine the position of frame markers in the data (*not shown; inherently there is a framer doing just that in the demultiplexer because on page 1625, last paragraph continues to page 1626, first paragraph, Yoshikawa discloses 48 Mb/s X 100 Mb/s of parallel data is grouped into 6 ch X 8 b.*)

Regarding **claim 57**, in addition to features recited in base claim 55 (see rationales discussed above), Yoshikawa further discloses wherein the demultiplexer is in a first node and the deskewing processor is in a second node, the first and second nodes communicating over parallel transmission link (MMF ribbon) (*see Fig. 1 for connection details*).

Regarding **claim 58**, in addition to features recited in base claim 57 (see rationales discussed above), Yoshikawa further discloses wherein the parallel transmission links comprise a parallel-optics based transmission link (MMF ribbon).

Regarding **claim 59**, in addition to features recited in base claim 57 (see rationales discussed above), Yoshikawa further discloses wherein the parallel transmission link comprises a wavelength division multiplexed (WDM) based (8X1.1 Gb/s O/E module) transmission link (MMF ribbon).

Regarding **claim 60**, in accordance with Yoshikawa reference entirety, Yoshikawa discloses a method (Fig. 1) for transferring synchronous optical network/synchronous digital hierarchy (SONET/SDH) frames (48bit X 100Mb/s), the system comprising:

mapping (Input: 48 bit X 100Mb/s) incoming frames of data having a given number of bits onto a plurality of data channels in a manner supporting de-skewing the data from the data channels (MMF ribbon) without increasing the given number of bits on the data channels (*see page 1626, right column pertaining the insertion of sync pattern to compensate for skewing*); and

de-skewing (*Fig. 1; Sync pattern extraction*) the data from the data channels (MMF ribbon) based on the mapped incoming frames (*see page 1626, right column pertaining the extraction of sync pattern performed by the deskewing operation*).

Regarding **claim 61**, in addition to features recited in base claim 60 (see rationales discussed above), Yoshikawa further discloses transmitting (*Fig. 1; 8 X 1.1 Gb/s E/O module*) the data channels via a parallel-optics based transmission link (MMF ribbon).

Regarding **claim 62**, in addition to features recited in base claim 61 (see rationales discussed above), Yoshikawa further discloses wherein the parallel-optics based transmission link uses at least twelve fibers (MMF ribbon).

Regarding **claim 63**, in addition to features recited in base claim 60 (see rationales discussed above), Yoshikawa further discloses wherein transmitting the data

channels include wavelength division multiplexing (WDM) (8X1.1 Gb/s O/E module) the data channels (MMF ribbon).

Regarding **claim 64**, in addition to features recited in base claim 60 (see rationales discussed above), Yoshikawa further discloses wherein the rate of SONET/SDH frames corresponds to an OC-192/STM-64 line rate (8 Gb/s) (*see Fig. 1 and 8 X 1.1 Gb/s array E/O transceiver modules*).

Regarding **claim 65**, in addition to features recited in base claim 60 (see rationales discussed above), Yoshikawa further discloses detecting a polarity of the transmission links by use of unique frame markers on subsets of the data channels (*see page 1626, right column, last paragraph pertaining the monitoring and detecting of the CRC bit*).

Regarding **claim 66**, in addition to features recited in base claim 60 (see rationales discussed above), Yoshikawa further discloses detecting and correcting errors on the data channels by calculating a cyclic redundancy check for a block of data on the data channels; comparing the CRC to a corresponding, separately-transmitted CRC for the block; and recovering the data from a protection channel if the CRC's do not match (*see page 1626, right column, last paragraph pertaining CRC bit*).

Response to Arguments

3. Applicant's arguments filed 07/03/06 have been fully considered but they are not persuasive.

In the Remarks of the outstanding response, on page 1, pertaining the rejection of

claim 1 under 35 U.S.C. §102(b) as being anticipated by Yoshikawa et al, Applicants states "*in an embodiment discussed at page 7, lines 20-23 of the specification as originally filed, each channel is encoded, and certain SONET framing bytes on each channel are overwritten with a frame marker consisting of characters defined for the node. The frame markers aid de-skewing circuitry at the receiver end as framing allows the receiver to realign the frames*" and argues the Yoshikawa reference does not teach "*a first de-skewing processor to overwrite a frame marker on the SONET/SDH frames with a unique frame marker to aid in de-skewing the plurality of data channel.*"

Examiner agrees the Yoshikawa's passage pointed out by the Applicants in the argument is different from that of the instant application specification disclosed on page 7, lines 20-23. However, Examiner respectfully disagrees with the Applicants' allegation that the Yoshikawa reference fails to teach the claimed limitation of "*a first de-skewing processor to overwrite a frame marker on the SONET/SDH frames with a unique frame marker to aid in de-skewing the plurality of data channel.*" On page 1626, left column, Yoshikawa clearly states "Skew was compensated using inserted sync pattern, which is a K28.5-characters generated in 8b10b coding. As clearly pointed out in the Office Action, the Sync Pattern Insertion circuit is corresponding to "a first de-skew process" and the action of "inserting" is corresponding to "overwrite" and "sync pattern" or "k28.5-characters is corresponding to "a frame marker" to aid deskewing at the receiver end. Even though the term "SONET/SDH" term is silent is the Yoshikawa reference, it is recognized or contemplated by those skilled in the art that Yoshikawa's data frame is a

SONET/SDH frame because it is commonly used in transporting data frame in an optical network such as Yoshikawa.

On page 3 of the outstanding Remarks, pertaining the rejection of claims 55 by the same reference above, Applicants argue "*Even though Independent claim 55 does not overwrite a frame marker as in claim 1, claim 55 does not anticipated by Yoshikawa ... Yoshikawa does not teach ... "a demultiplexer to map incoming frames of data having a given number of bits onto a plurality of data channels.*"

Examiner respectfully disagrees with the Applicants' argument. Claim 55, in the present condition, is rather broad. It merely calls for a circuitry that performs a technique commonly know as data stripping in a multichannel optical network. Yoshikawa as clearly pointed out in the Office Action does indeed disclose such claimed limitation. On page 1626, pertaining the inserting of sync pattern to skew compensate, Yoshikawa clearly states "*After 8b10 coding, the coded 6 X 10 bit data was 60:6 multiplexed and transmitted through a GI/62.5 MMF ribbon by using 8X 1 Gb/s array optical module*". This operation is reversed at the receiving end in the 1:10 multiplex circuit. The recitation thereat clearly anticipates the claimed limitations in the present condition.

Perhaps, in a response to this Office Action, Applicants should further amend the claims to better reflect the disclosed invention as well as further distinguish the claimed invention from that taught by Yoshikawa and the existing arts.

Examiner believes an earnest attempt has been made in fully addressing all of the Applicants' arguments. Due to the arguments are not persuasive and the

communications failed 07/03/06 fails to place the instant application in a favorable condition for allowance, the rejection is maintained.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yoshikawa et al, Gbyte-Class Skewless Parallel-Optical-Data-Link Subsystem, IEEE, pages 63-64, 1996.

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Frank Duong whose telephone number is 571-272-3164. The examiner can normally be reached on 7:00AM-3:30PM, Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ahmad Matar can be reached on 571-272-7488. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

FRANK DUONG
PRIMARY EXAMINER

September 17, 2006